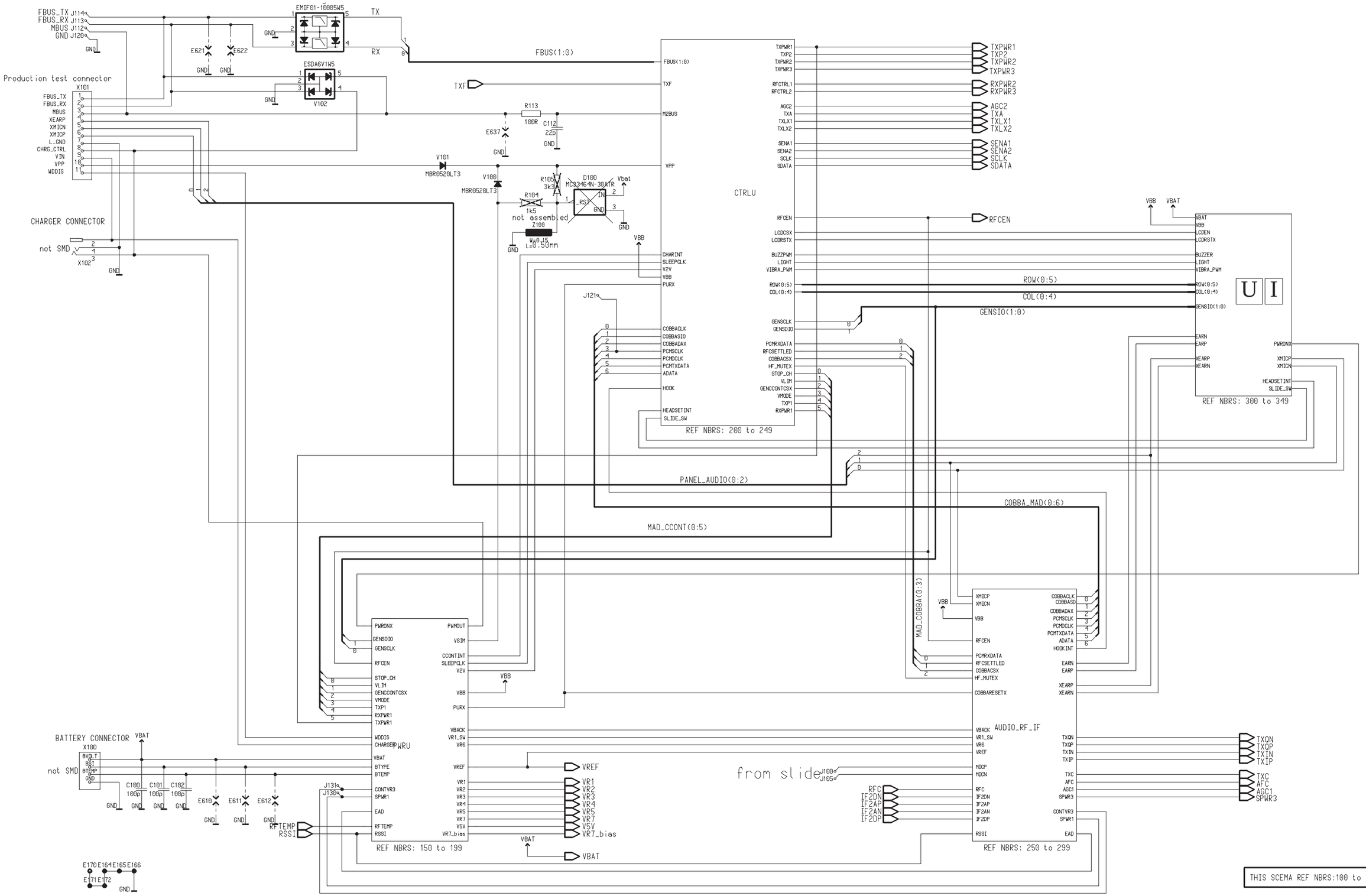
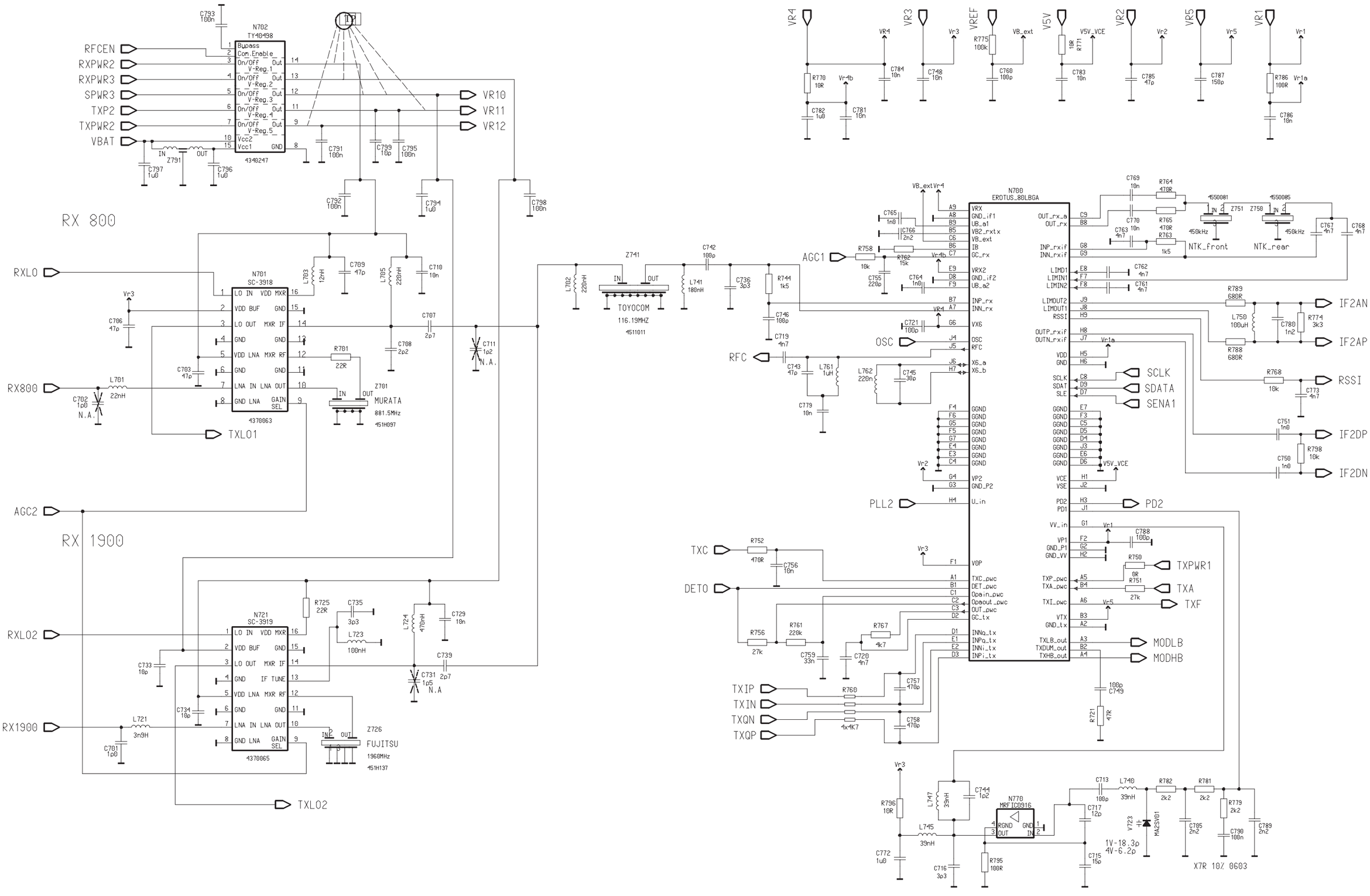
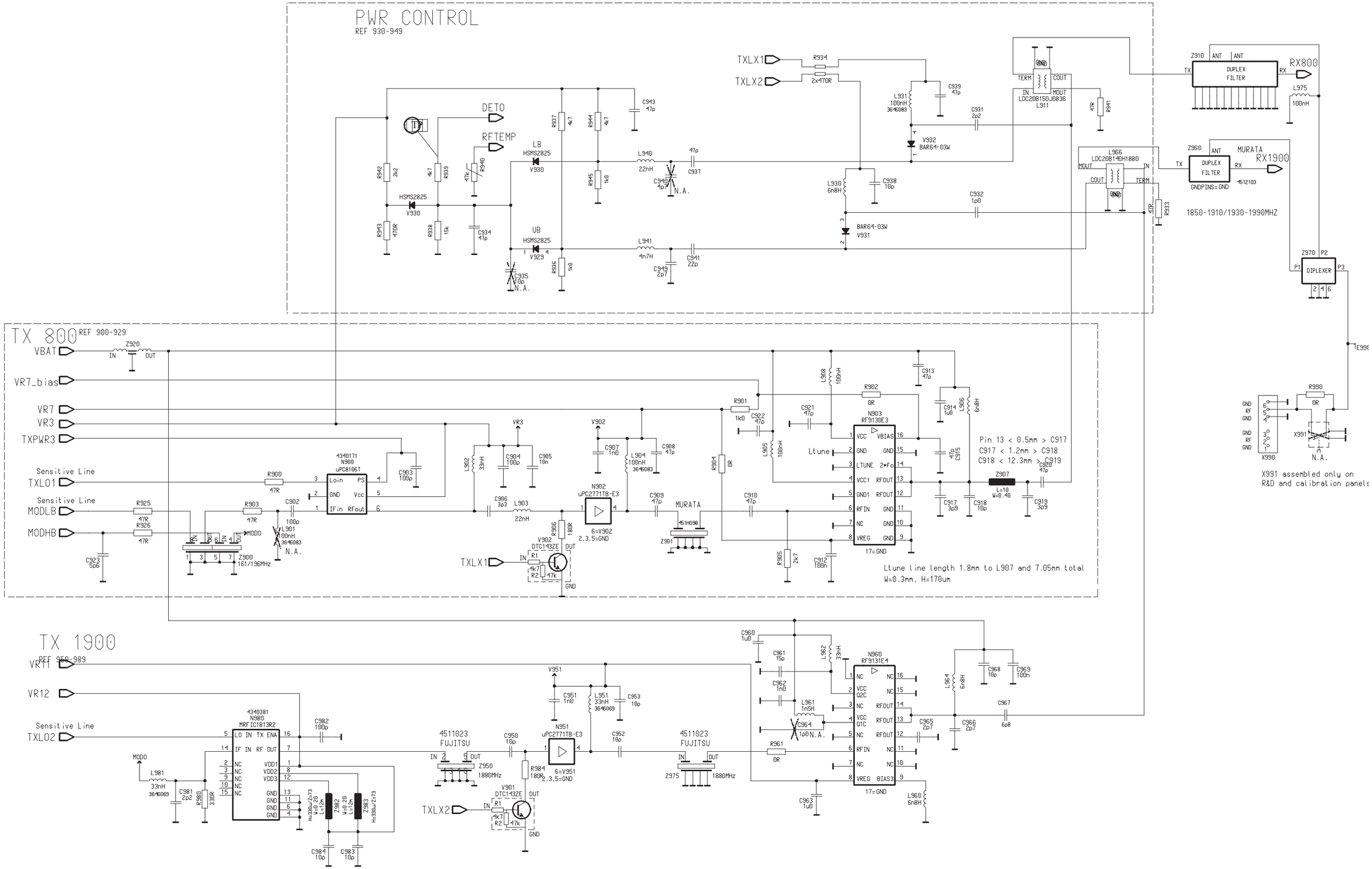
Block Diagram of SE2 Module (Version 5100 Edit 120)



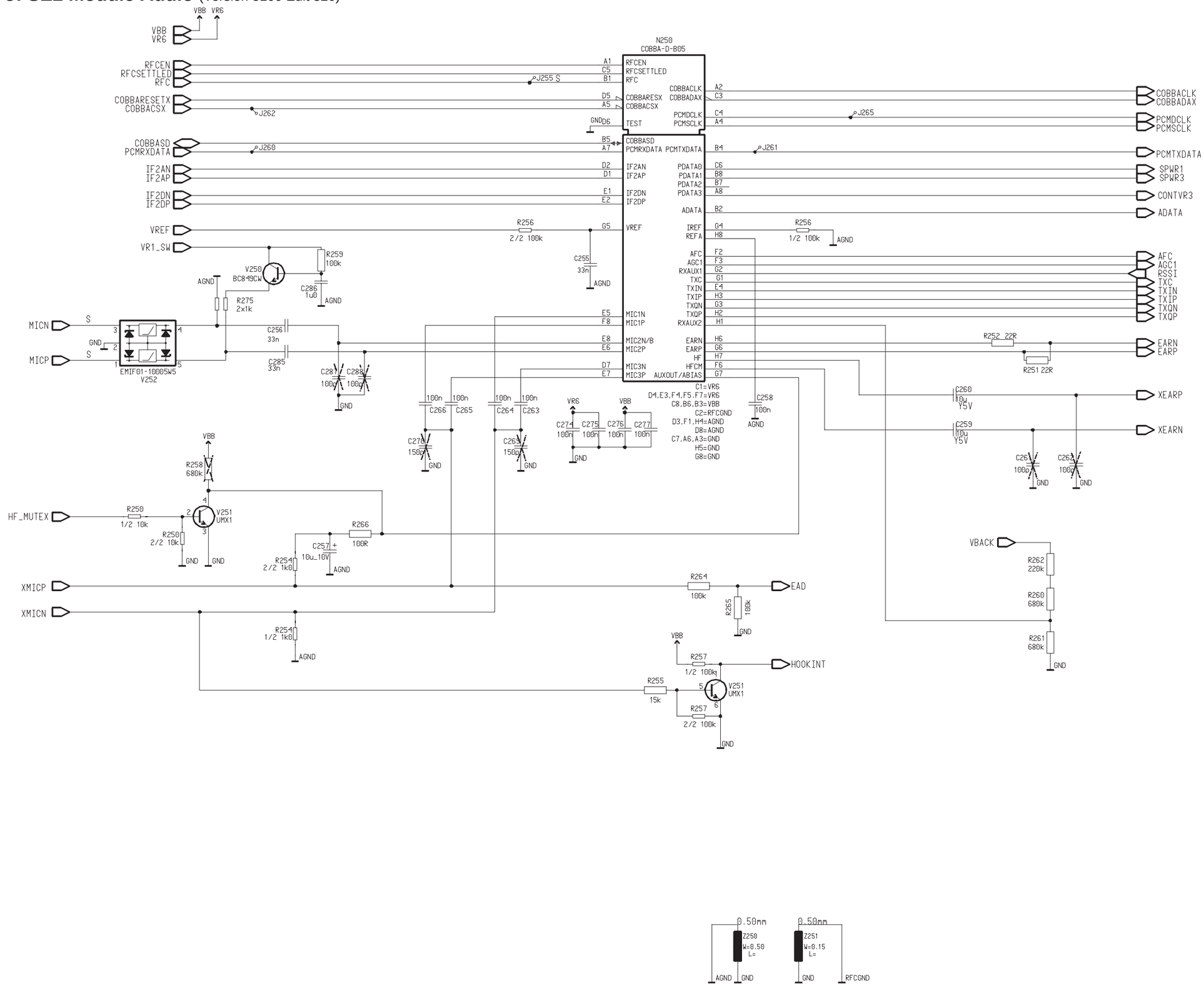
Circuit Diagram of SE2 Module RX (Version 5100 Edit 236)



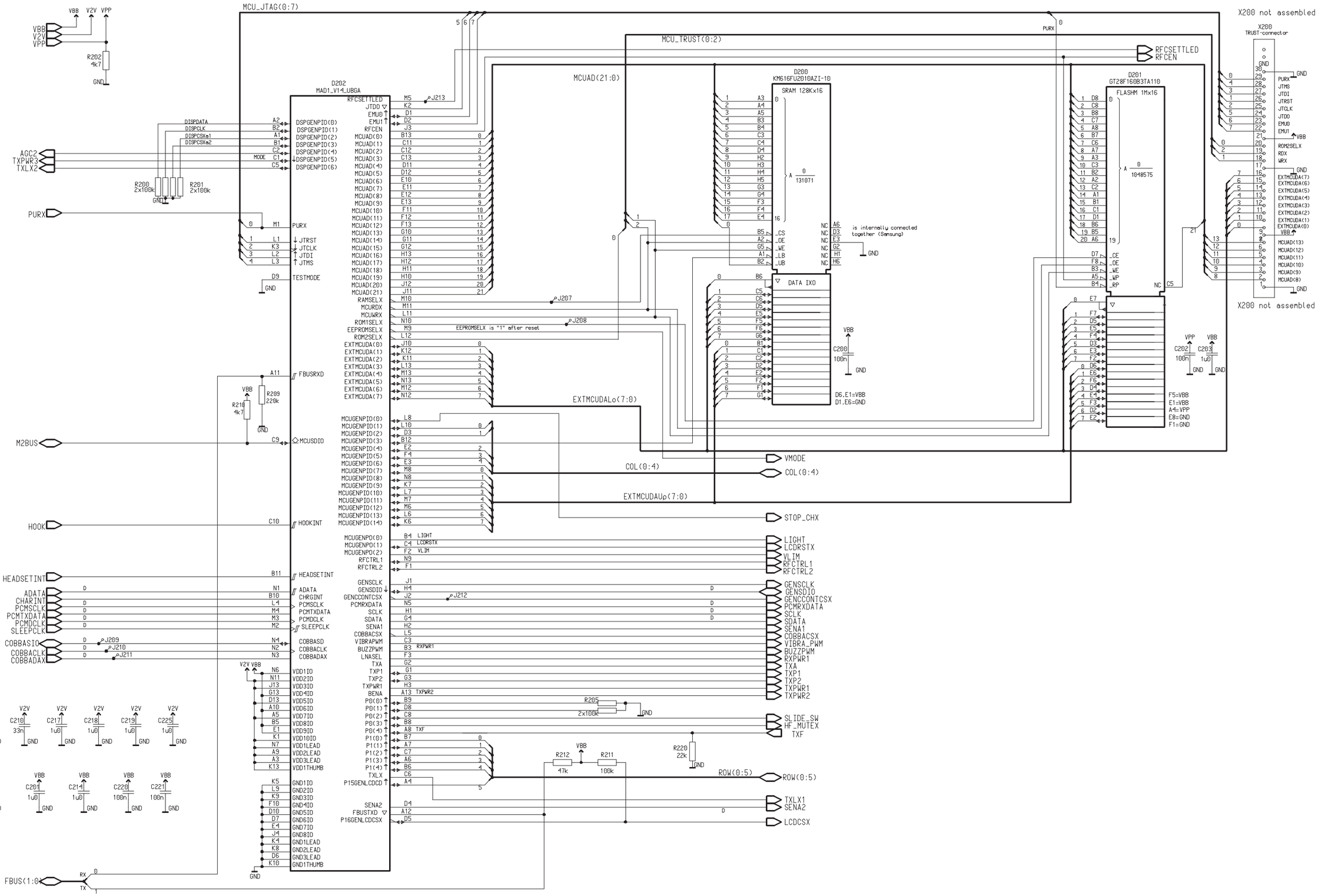
Circuit Diagram of SE2 Module TX (Version 5100 Edit 573)



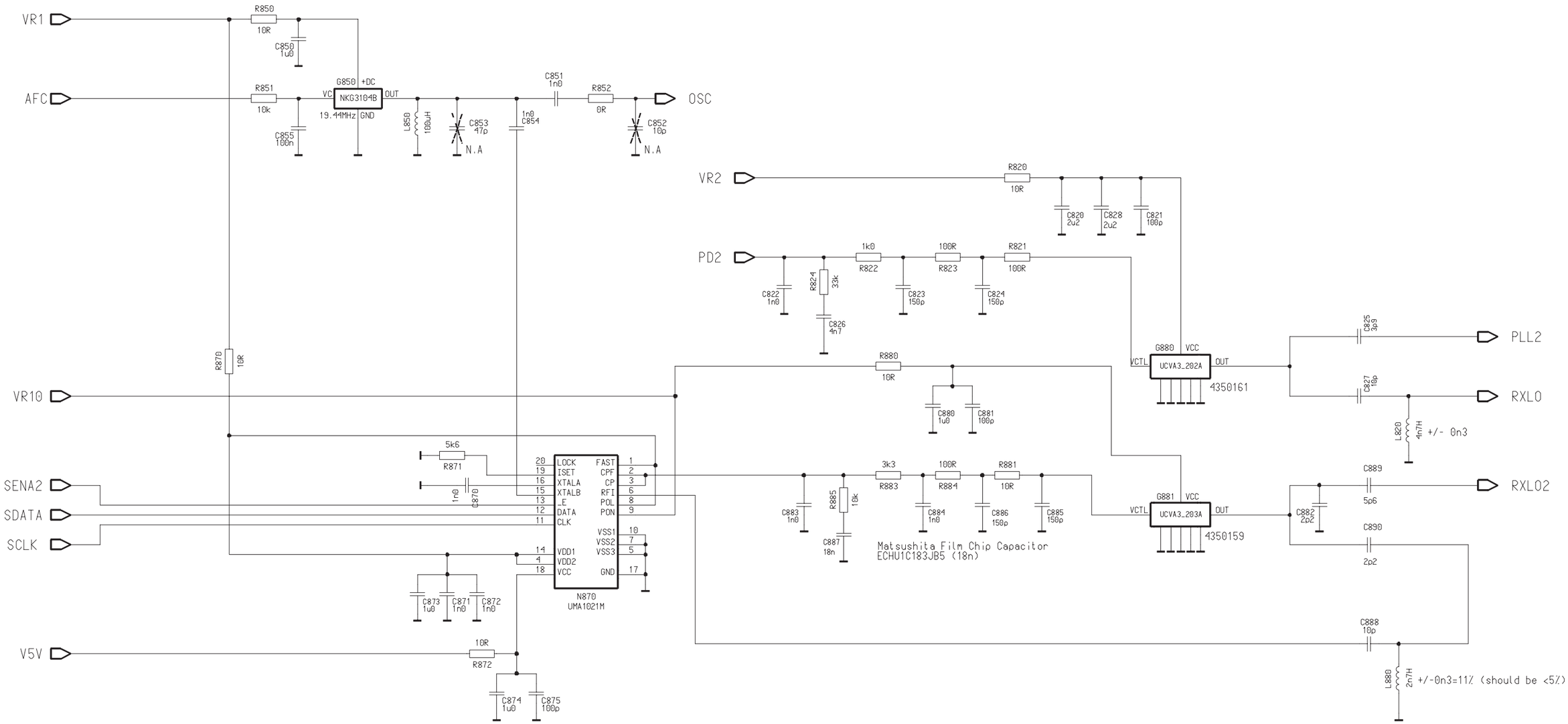
Circuit Diagram of SE2 Module Audio (Version 5100 Edit 320)



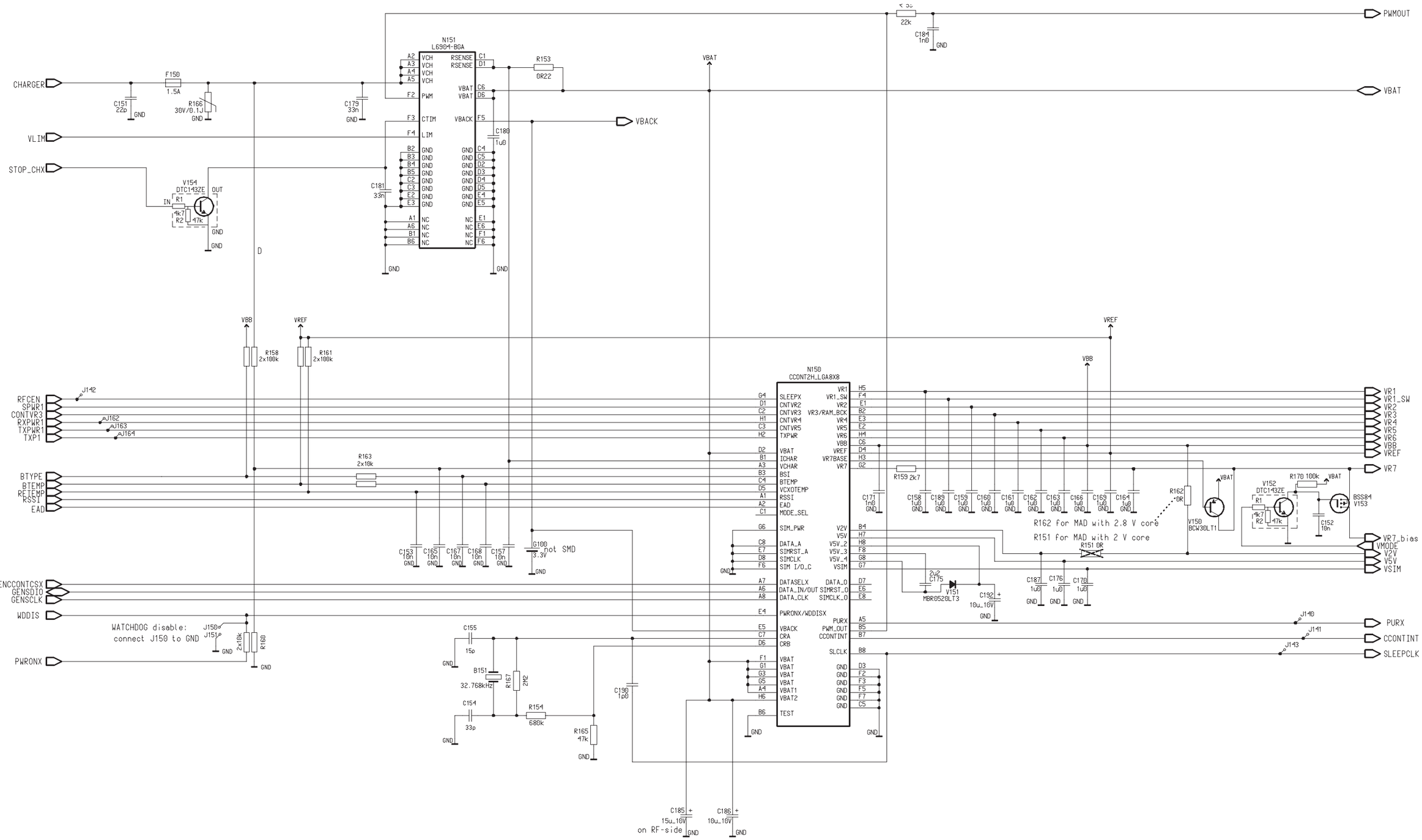
Circuit Diagram of SE2 Module CTRLU (Version 5100 Edit 406)



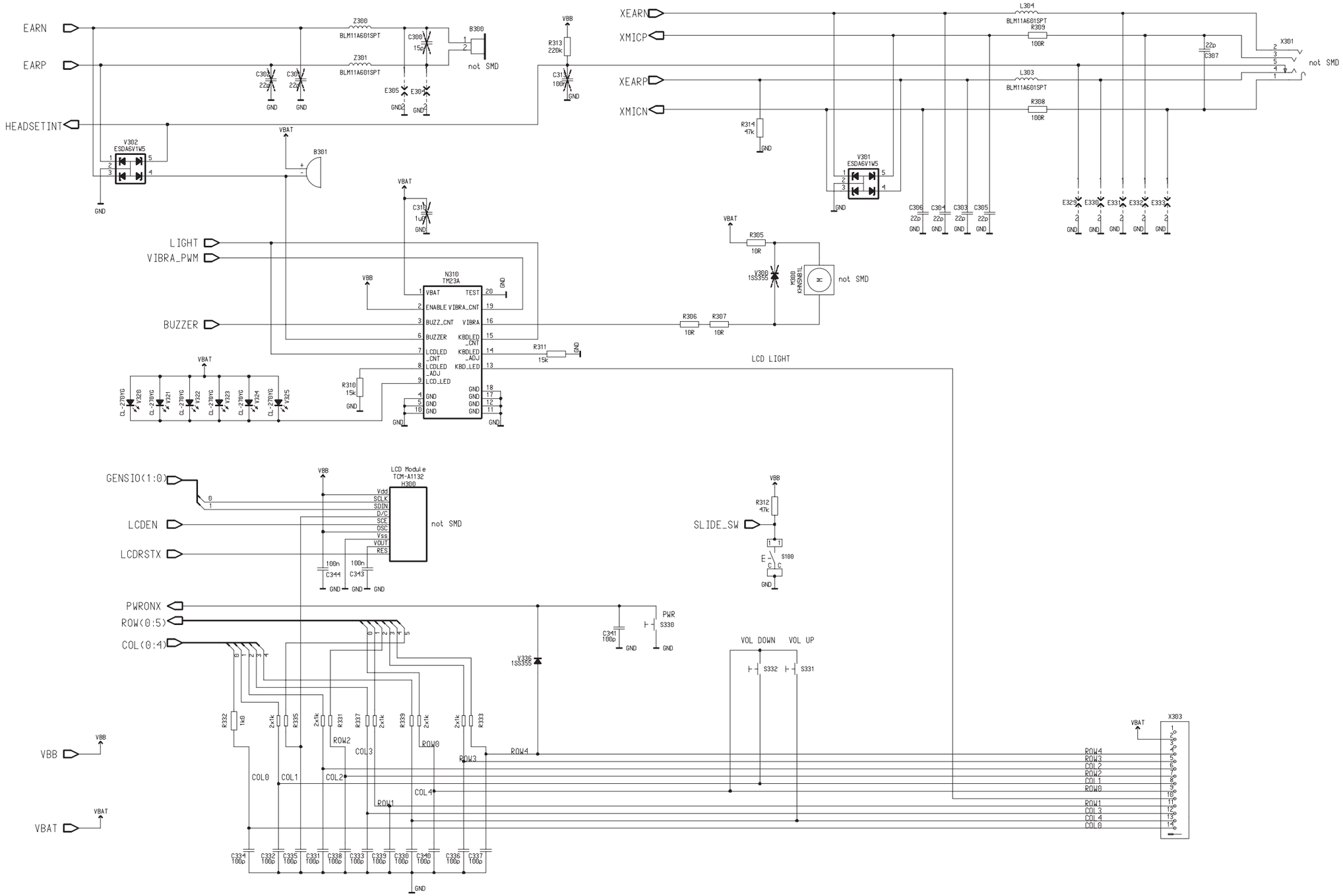
Circuit Diagram of SE2 Module Synthesizer (Version 5100 Edit 195)



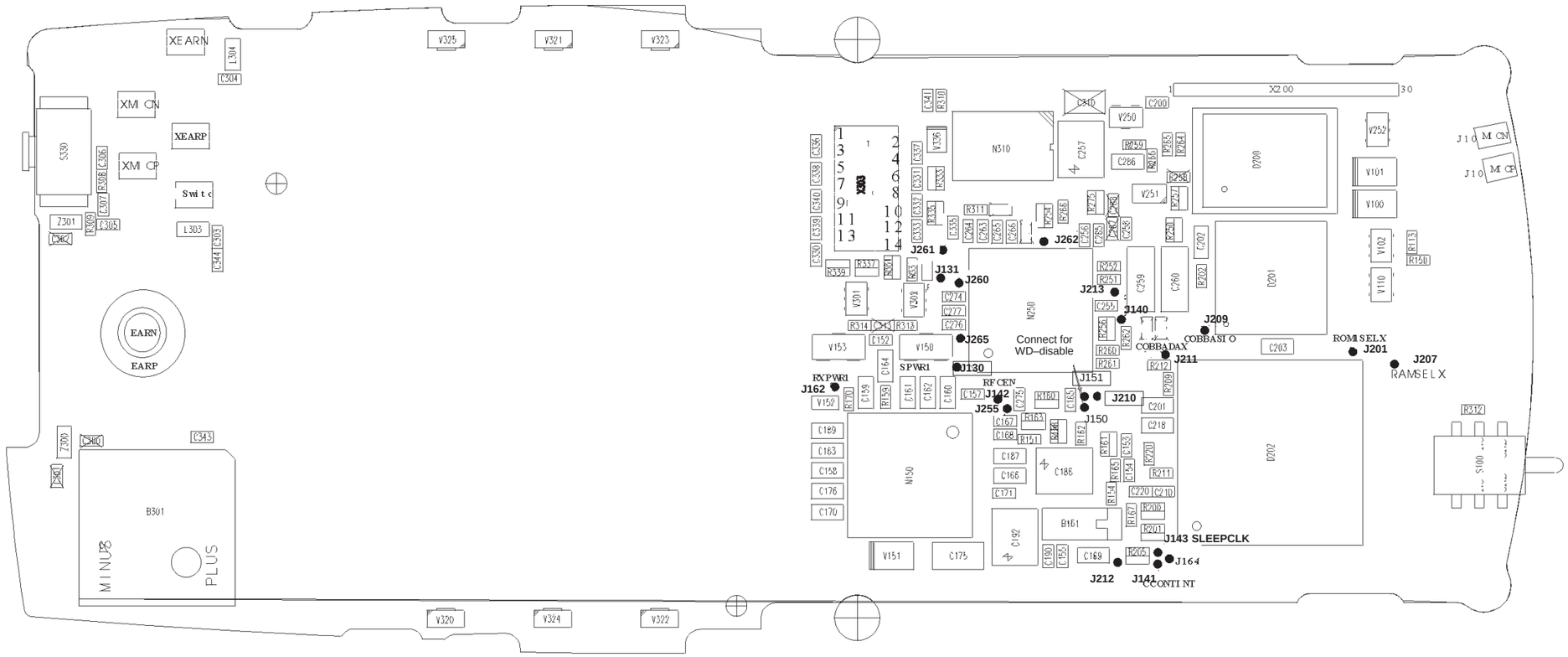
Circuit Diagram of SE2 Module PWRU (Version 5100 Edit 409)



Circuit Diagram of SE2 Module User interface (Version 5100 Edit 180)



Parts Placement Diagram of SE2 Module (Version 10_v3) 1/2

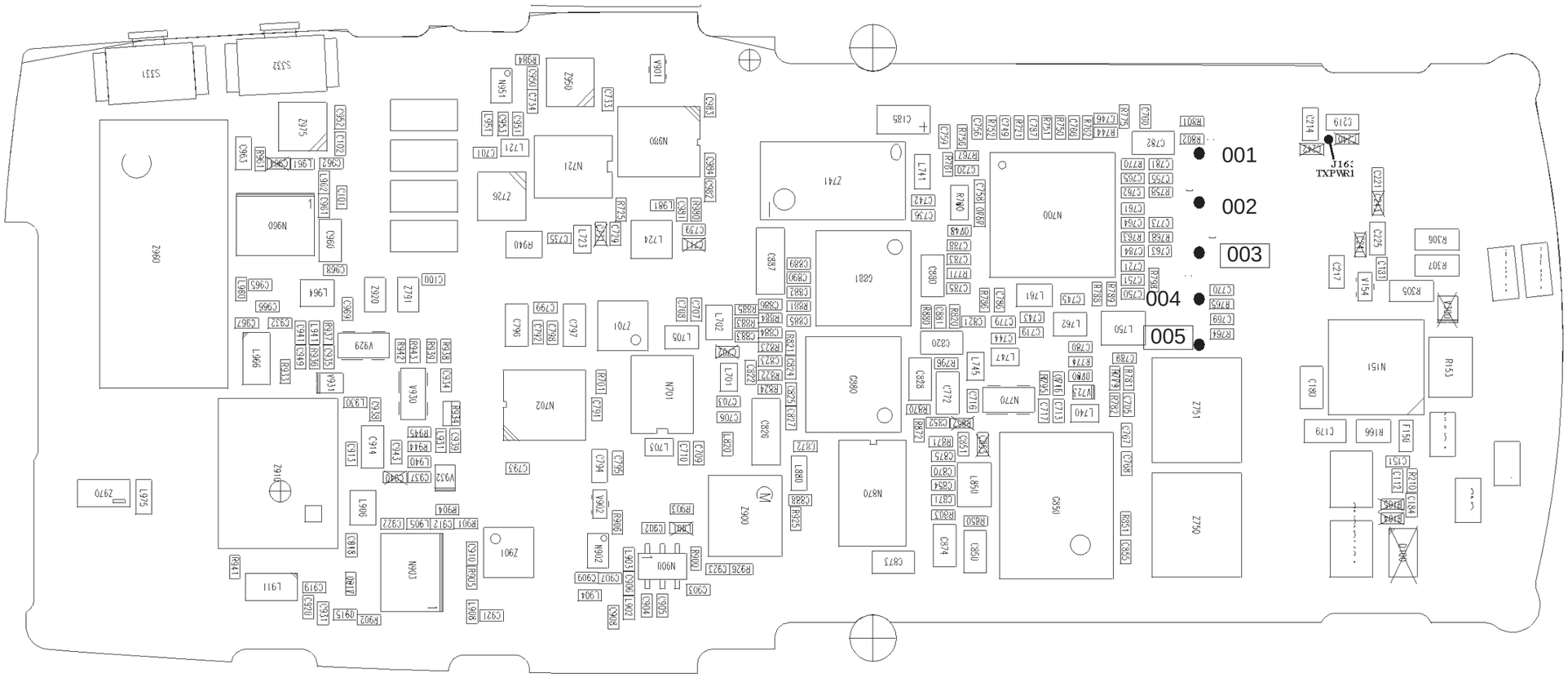


Test point description

Test point	Name	From–to	Level	Description
J121	PCMSCLK	COBBA A4– MAD L4		8.0 kHz (digital), 8.1 kHz (analog)
J140	PURX	CCONT A5–MAD M1, D201 B4, COBBA D5	Reset state 0V, normal state 2.8V	RESET power up/down
J141	CCONTINT	CCONT B7–MAD B10	Pulse active 2.8V, non–active 0V	Charger interrupt
J142	RFCEN	MAD J3– D201 A5, CCONT G4	Pulse active 2.8V, non–active 0V	Active state
J143	SLEEPCLK	CCONT B8– MAD M2	Pulsed DC < 0.8V/>2.4V	32.768 kHz, power on
J150	WDDIS/PWRONX	X101–CCONT E4	Pulse active 0V, non–active 2.8V	Watchdog disable
J151	GND	J156–GND		Ground for WDDIS

J207	RAMSELX	MAD M10– D200 B5		
J208	ROM1SELX	MAD N10– D201 D7		
J209	COBBASIO	MAD N4– COBBA B5		Bidirectional data line
J210	COBBACLK	COBBA A2– MAD N2	Pulsed DC (<0.5V/>2.15V)	COBBA system clock
J211	COBBADAX	MAD N3– COBBA C3		Data ready flag
J212	DATASELX	MAD J2– CCONT A7		Read/write enable
J213	RFCSETTLED	MAD M5– COBBA C5	Pulse active 2.8V, non–active 0 V	Active state
J262	COBBACSX	MAD L5– COBBA A5		Chip select
J255	RFC	EROTUS 25– COBBA B1	0.7 Vpp sinewave	19.44 MHz clock
J260	PCMRXDATA	MAD N5– COBBA A7		Receive data line
J261	PCMTXDATA	COBBA B4– MAD M4		Transmit data line
J265	PCMDCLK	COBBA C4– MAD M3		1.08 MHz (digital), 1.215 MHz (analog)

Parts Placement Diagram of SE2 Module (Version 10_v3) 2/2



Test point	Name	From–to	Level	Description
J163	TXPWR1			
001	PCMSCLK			
002	L–GND			
003	FBUS–TX			
004	FBUS–RX			
005	MBUS			